In the Abstract

Delete the existing Abstract and substitute the following in its place:

DRAM circuitry includes an array of word lines forming gates of field effect transistors and an array of bit lines. Individual field effect transistors include a pair of source/drain regions. A plurality of memory cell storage capacitors are associated with the field effect transistors. Individual storage capacitors include a first capacitor electrode in electrical connection with one of a pair of source/drain regions of one of the field effect transistors and a second capacitor electrode. A capacitor dielectric region is received intermediate the first and second capacitor electrodes. The capacitor dielectric region includes aluminum nitride. The other of the pair of source/drain regions of the one field effect transistor are in electrical connection with one of the bit lines.